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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/887,783	CHENG ET AL.
	Examiner	Art Unit
	Cynthia Britt	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-68 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4,7-12,14-18,21-26,28-46,49-54,56-60 and 62-68 is/are rejected.

7)☒ Claim(s) 1-7,9-21,23-35,38-49,51-56,59-61,63,65,67 and 68 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 June 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-68 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on August 27, 2001 has been considered by the examiner.

Allowable Subject Matter

Claims 4-6,13, 18-20, 27, 46-48, 55, 61, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and nay objections and any 35 U.S.C. 112 second paragraph issues are overcome.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 29-42 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. (See MPEP 2106 IV B 1. (a) (p. 2100-13))

(a) Functional Descriptive Material: "Data Structures" Representing Descriptive Material Per Se or Computer Programs Representing Computer Listings Per Se Data structures not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the

computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention, which permit the data structure's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory. ... Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer, which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program (such as claims 43-56 of the present application) is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory.

Claim Objections

Claims 1-7, 9-21, 23-35, 38-47, 49, 51-56, 59-61, 63, 65, 67, and 68 are objected to because of the following informalities:

In line 9 of claim 1 the nonfunctional term "whereby" is used.

In line 3 of claim 2 the nonfunctional term "wherein" is used.

In line 1 of claim 3 the nonfunctional term "wherein" is used.

In line 4 of claim 3 the nonfunctional term "whereby" is used.

In line 1 of claim 4 the nonfunctional term "wherein" is used.

In lines 3, 8, and 11 of claim 4 the nonfunctional term "whereby" is used.

In line 1 of claim 67 "where in" is intended to be "wherein".

In line 6 of claim 67, "transfersthe" should be "transfers the".

Although all claims containing this "whereby or wherein" informality are not listed specifically, applicant should consider terms such as "configured to" or "connected such that" in order to clarify the limitations of the claim. The examiner would like to remind applicant that language that suggests or makes optional but does not require steps to be preformed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The terms "wherein" and " whereby" are recited in many of the claims in this application. See MPEP 2106 II C (page 2100-8). Such recitation is non- functional language, and as a result, is not given patentable weight. *It has been held that functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish in re Mason, 114 USPQ, 44 CCPA 937 (1957)*

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 10, 12, 18, 24, 26, 32 38, 40, 46, 52, 54, 60, 61, 63, and 67, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to

particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "each subsequent flip circuit" in line 8. It is unclear what a "flip circuit" would be used to accomplish. The examiner will assume for the purpose of examination that "flip circuit" should be "flip-flop circuit".

Claim 10 recites the limitation "the RAM data" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the RAM" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the PASS/FAIL signal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites the limitation "each subsequent flip circuit" in line 8. It is unclear what a "flip circuit" would be used to accomplish. The examiner will assume for the purpose of examination that "flip circuit" should be "flip-flop circuit".

Claim 24 recites the limitation "the RAM data" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 26 recites the limitation "the RAM" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 26 recites the limitation "the PASS/FAIL signal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 32 recites the limitation "each subsequent flip circuit" in lines 8-9. It is unclear what a "flip circuit" would be used to accomplish. The examiner will assume for the purpose of examination that "flip circuit" should be "flip-flop circuit".

Claim 38 recites the limitation "the RAM data" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 40 recites the limitation "the RAM" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 40 recites the limitation "the PASS/FAIL signal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 46 recites the limitation "each subsequent flip circuit" in lines 8-9. It is unclear what a "flip circuit" would be used to accomplish. The examiner will assume for the purpose of examination that "flip circuit" should be "flip-flop circuit".

Claim 52 recites the limitation "the RAM data" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 54 recites the limitation "the RAM" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 54 recites the limitation "the PASS/FAIL signal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 60 recites the limitation "parallel to parallel converter" in line 2. It is unclear to the examiner why a "parallel to parallel converter" would be necessary, or what it would be used to accomplish. For the purpose of examination, the examiner will

assume that applicant intended "parallel to parallel converter" to be "parallel to serial converter".

Claim 61 recites the limitation "each subsequent flip circuit" in line 8. It is unclear what a "flip circuit" would be used to accomplish. The examiner will assume for the purpose of examination that "flip circuit" should be "flip-flop circuit".

Claim 63 in line 1, recites the limitation "said comparator". There is insufficient antecedent basis for this limitation in the claim.

Claim 63 recites the limitation "the RAM data" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 67 recites the limitation "the RAM" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 67 recites the limitation "the PASS/FAIL signal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 8-12, 14-17, 22-26, 28, 43-45, 50-54, 56-59, and 62-68, are rejected under 35 U.S.C. 102(e) as being anticipated by Rajsuman et al. U.S. Patent No 6,249,893.

As per claims 1, 15, 43, and 57, Rajsuman et al. teach a system and method of testing embedded cores in an integrated circuit chip having a microprocessor core, a memory core and other functional cores following the steps of: providing a plurality of registers to be used for testing the microprocessor core in the integrated circuit chip; testing the microprocessor core by executing its instructions multiple times under pseudo random data and evaluating the results by comparing simulation results; using an assembly language test program running on the microprocessor core to generate a memory test pattern by the microprocessor core using LFSR and MISR; applying the memory test pattern to the memory core by the microprocessor core and evaluating the response of the memory core by the microprocessor core; and testing the other functional cores by applying a function specific test pattern by the microprocessor core and evaluating the resultant output signals of the functional cores. Instruction decode logic generates function select and control signals for the instruction execution unit. Instruction decode logic generates function select and control signals for the instruction execution unit. To avoid the unknown data in a pipeline of the execution unit the start signal for MISR should be delayed by a time equal to (or more) the latency of pipeline. According to the algorithm of the test pattern, write data is written in the specified addresses of the memory core. The microprocessor core reads the stored data in the

memory core to compare the same with the original test data (column 3 lines 32-45, column 4 lines 64-66, column 7 lines 13-25,column 9 lines 4-12, figure 5C, 6A, 6B, 9).

As per claims 2, 16, 44, 58, 59, 64, and 65, Rajsuman et al. disclose test patterns require serialization (parallel to serial conversion) of the ALPG patterns, and also based upon implementation, it can be either parallel load or serial load (such as scan-in). It can be either a serial input or parallel input type; however, the parallel input type will cause a large number of wires to become primary input at the chip-level. The serial input implementation will require only one wire to be primary input. If it is implemented as a serial input type, it will also require a mode select signal to switch it from serial-in to parallel-out and vice-versa. (FIG. 5A, column 6 lines 1-23 and 58-65, column 2 line 18-24)

As per claims 3, 17, and 45, Rajsuman et al. teach that the instruction fetch unit obtains the opcode of the next instruction based upon the address in the program counter. This opcode is decoded by the instruction decode logic, which generates function select and control signals for the instruction execution unit. The instruction execution unit also receives the operand (data enters or results from the operation). Based upon these control signals, one of the logic blocks within the instruction execution unit computes its function. The operand or data for this computation are obtained from the system memory. For testing the microprocessor core, this general structure has been modified by three registers and two multiplexers to use extra registers to scan-in one instruction execute it multiple times with pseudo random data and take out the resultant signature. The Test Control Register is used to provide the

opcode of microprocessor's instructions during the test mode. Failed tests are reported to the host computer. (FIG. 2 column 4 line 63 through column 5 line 25, column 11 lines 51-56)

As per claims 8-12, 22-26, 50-54, 62, 63, 66, and 67, Rajsuman et al. teach that the microprocessor core generates a test pattern from the object code. These test patterns are applied to the memory core. According to the algorithm of the test pattern, write data is written in the specified addresses of the memory core. The microprocessor core reads the stored data in the memory core to compare the same with the original test data prepared by the microprocessor core, which is typically the write data. When the data read from the memory core does not match the expected data, failure information is sent to the host computer. An example assembly language procedure using simplified memory marching algorithm is shown in FIGS. 10A and 10B. The marching pattern in FIGS. 10A and 10B is used only for an illustration purpose, and any algorithm can be used. The test program may stop as soon as an error occurs. The host computer or IC tester immediately observes the failure and hence, fail-bit location is immediately known. A user can modify the program in various ways to collect any desired test information of the embedded memory. It is also well known in the testing industry to use 'exclusive OR' circuitry for comparison (column 9 lines 1-35,).

As per claims 14, 28, 56, and 68, Rajsuman et al. teach a method and structure for testing embedded cores based system-on-a-chip, and more particularly, to a method and structure for testing microprocessors, microcontrollers, memories and other

functional cores embedded in a large scale integrated circuit (LSI) such as a system-on-a-chip (SoC) IC. (Column 1 lines 6-11)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 7, 21, 49, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajsuman et al. U.S. Patent No. 6,249,893 in view of Whetsel U.S. Patent No. 6,499,070.

As per claims 7, 21, 49, and 60, Rajsuman et al. substantially teach the claimed system and method of testing embedded cores in an integrated circuit chip having a microprocessor core, a memory core and other functional cores following the steps of: providing a plurality of registers to be used for testing the microprocessor core in the integrated circuit chip; testing the microprocessor core by executing its instructions multiple times under pseudo random data and evaluating the results by comparing simulation results; using an assembly language test program running on the microprocessor core to generate a memory test pattern by the microprocessor core using LFSR and MISR; applying the memory test pattern to the memory core by the microprocessor core and evaluating the response of the memory core by the microprocessor core; and testing the other functional cores by applying a function specific test pattern by the microprocessor core and evaluating the resultant output signals of the functional cores. Instruction decode logic generates function select and control signals for the instruction execution unit. Instruction decode logic generates function select and control signals for the instruction execution unit. To avoid the unknown data in a pipeline of the execution unit the start signal for MISR should be delayed by a time equal to (or more) the latency of pipeline. According to the algorithm of the test pattern, write data is written in the specified addresses of the memory core. The microprocessor core reads the stored data in the memory core to compare the

same with the original test data (column 3 lines 32-45, column 4 lines 64-66, column 7 lines 13-25,column 9 lines 4-12, column 6 lines 1-23 and 58-65 figure 5A-5C, 6A, 6B, 9). Not explicitly disclosed is the makeup of the parallel to serial converter using a plurality of flip-flop circuits with a plurality of multiplexer circuits.

However, in analogous art, Whetsel teaches parallel to serial conversion using a plurality of flip flop (or latch) circuitry along with a multiplexer circuit, these circuits implement a clocking signal and a select signal (Column 1 lines 28-40, column 7 lines 22-63). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the parallel to serial converter of Whetsel within the testing circuitry of Rajsuman et al. This would have been obvious as suggested by Rajsuman et al. Due to the multiplexer at the I/Os, the actual test patterns require serialization (parallel to serial conversion) of the ALPG patterns (FIG. 5A, column 2 line 18-24). It has also been held that mere duplication of the essential working parts of a device involves only routine skill in the art (St Regis Paper Co. v Bemis Co. 193 USPQ 8 7th Cir. 1977).

Claims 1, 15, 43, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crouch et al U.S. Patent No. 5,617,531 in view of Conner U.S. Patent No. 5,794,175.

As per claim 1, Crouch et al. substantially teach the claimed circuit which contains an internal test controller of a data processor, where the data processor includes a plurality of embedded memories. The internal test controller has a test pattern generator that generates a test pattern for each embedded memory within the

plurality of embedded memories and sequentially provides the test pattern to each embedded memory of the plurality of embedded memories. The internal test controller also has a memory verification element that is operably coupled to the test pattern generator. The memory verification element is used to verify integrity of the plurality of embedded memories in response to the plurality of embedded memories processing the test pattern. (Column 4 lines 12-24) Not explicitly disclosed is the latency buffers that adjust in time the relationship of the test signals.

However, in an analogous art, Conner teaches a system which during testing, will introduce delay in variable amounts into control signals in order to synchronize (column 3 lines 62-67). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the delay method of Conner with the testing system of Crouch et al. This would have been obvious in order to provide testing accuracy as suggested by Conner (column 2 lines 63-66).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,415,408 Rhodes et al.

This patent shows a circuit in which component 230i, in FIG. 17A, is a latency buffer, which has a pair of inputs D1 and D2, and a corresponding pair of outputs Q1 and Q2. Input D1 receives the parallel output signals from register 230g, and input D2 receives the parallel output signals from register 230h. The signals on the D1 and D2

inputs are stored in the latency buffer 230i in response to each positive edge of a clock signal. Those stored signals are subsequently regenerated on the outputs Q1 and Q2 after a predetermined number of cycles of the clock signal. Component 230j, in FIG. 17B, is a register which has a data input D and an output Q. The data input D receives the PAGE field that is in word W1 of instruction, (shown in FIG. 15G). Component 230m, in FIG. 17B, is a register, which has a data input D, an output Q, and a load control input. (Table 5 figures 17A&B column 35)

U.S. Patent No. 5,748,640 Jiang et al.

This patent teaches a processing unit having a CPU core, an integrated RAM and a test unit, which may be implemented in either a test unit, and implemented in either hardware or software. A built-in self-test of the RAM is designed to run concurrently with the functional vectors used to test the CPU core. Once the core tests have been activated, a control register may be written to by which will activate the built-in self-test. Thus, the BIST and core testing may overlap to minimize test time.

U.S. Patent No. 5,970,073 Masuda et al.

This patent teaches a test pattern generator circuit with a parallel/parallel-serial conversion means having a buffer memory for storing parallel data for four words delivered from the deploying means, a selector for selecting a first and a third word during a first and a second test cycle from the parallel data for a first to a fourth word which occur every period of 2T in the buffer register, and a selector for selecting a second and a fourth word during the first and the second test cycle. (Figure 3 claims 1 and 2)

"Processor-Based Built-In Self-Test for Embedded DRAM" by Dreibelbis et al. Microelectron. Div., IBM Corp., Essex Junction, VT, USA; *This paper appears in:* IEEE Journal of Solid-State Circuits, Publication Date: Nov. 1998 On page(s): 1731 - 1740 Volume: 33 , Issue: 11 ISSN: 0018-9200 Inspec Accession Number: 6087324

This paper teaches a built-in self-test engine and test methodology which have been developed for testing a family of high-bandwidth, high-density DRAM macros. The DRAM macros range in size from 256×16×128 to 2 K×16×256 (Word×Bit×Data) and are targeted for embedded applications in application-specific integrated circuit designs. The processor-based test engine, with two separate instruction storage memories, combines with flexible address, data, and clock generators to provide DRAM high-performance ac testing using a minimum of dedicated test pins. Test results are compressed through on-macro, two-dimensional, redundancy allocation logic to provide direct programming information for the fuser via a serial scan port.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

Cynthia Britt
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100